Claims

1. A circuit arrangement for operating discharge lamps, having the following features:

   - power factor correction device which oscillates with a PFC clock cycle and provides an intermediate circuit voltage,

   - inverter which oscillates with an inverter clock cycle which is independent of the PFC clock cycle, draws its power from the intermediate circuit voltage and is capable of outputting power to discharge lamps ,

   - an oscillation of the power factor correction device is started, by means of a starting device , by an oscillation of the inverter .

2. The circuit arrangement as claimed in claim 1, comprising an overvoltage shutdown which stops the oscillation of the power factor correction device when the intermediate circuit voltage exceeds a predetermined overvoltage threshold.

3. The circuit arrangement as claimed in claim 2, comprising a fault shutdown which stops the oscillation of the inverter in the event of a fault.

4. The circuit arrangement as claimed in claim 2, where the overvoltage shutdown operates in a monostable manner.

5. The circuit arrangement as claimed in claim 3, where the overvoltage shutdown operates in a monostable manner and the fault shutdown operates in a bistable manner.

6. The circuit arrangement as claimed in claim 4 or 5, where the overvoltage shutdown stops the power factor correction device for at least 100 microseconds when the intermediate circuit voltage exceeds a predetermined overvoltage threshold.

7. The circuit arrangement as claimed in claim one, where the power factor correction device is a self-oscillating step-up converter having a step-up converter switch , a step-up converter inductor and a step-up converter diode , the voltage across the step-up converter switch forming a feedback variable.

8. The circuit arrangement as claimed in claim 7, where the output of the inverter is capacitively coupled to the feedback variable.

9. The circuit arrangement as claimed in claim 8, where the inverter is a half-bridge inverter having two half-bridge switches (T3, T4), the tie point of the half-bridge switches (T3, T4) being coupled to the tie point of the step-up converter inductor and the step-up converter diode via a trigger capacitor .

10. The circuit arrangement as claimed in claim 9, where the half-bridge inverter is self-oscillating.